VIDEO A-D/D-A CONVERTER

PART 1: INTRODUCING THE ICs

Although fast 8-bit video converters are available from a variety of manufacturers, their practical application has so far been over the head of the average electronics hobbyist with an interest in video signal processing. Fortunately, that situation has come to an end with the introduction of a number of simple to use A-D and D-A converter ICs from Philips Components. Two of these ICs, the TDA8708 ADC and the TDA8702 DAC, form the heart of an advanced video converter described in this two-instalment article. This month we discuss the basic operation of ADC and the DAC, followed next month by a constructional project intended to get you going with video encoding/decoding experiments, digital video processing, sync locking techniques, etc.

P. Godon (Philips Components, Paris)

TDA8708 analogue-to-digital converter

The TDA8708 contains more than just a fast ADC — in fact, it should be referred to as a 'video analogue input interface'. The internal diagram of the TDA8708, which is also available in a surface-mount assembly package (suffix -T), is given in Fig. 1. Clearly, the ADC is but one of a number of functional blocks contained in the IC. Each of the three analogue video inputs, VIN0, VIN1 and VIN2 may be driven by a CVBS (chrominance-video-blanking-synchronization) signal of an average level between 0.45 V and 1.6 V measured with respect to the analogue ground, AGND. The typical input capacitance of the VINx inputs is about 1 pF, while the input impedance lies between 10 kΩ and 20 kΩ (input capacitance and input impedance values without external components). The video input selection is effected by applying logic levels to the I0 and I1 inputs of the chip as shown below:

Table 1. Input channel selection

I1	I0	VINx
0	0	0
0	1	1
1	0	2
1	1	2

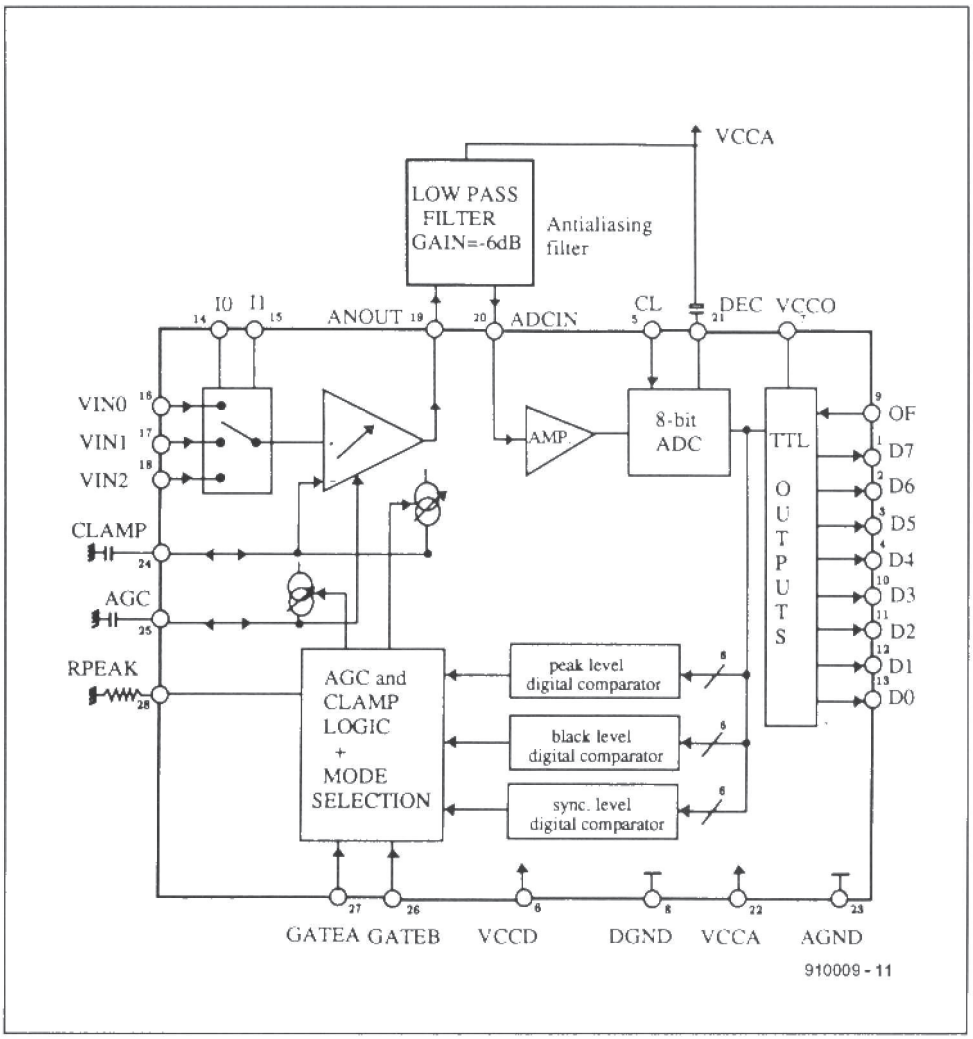

Fig. 1. Internal diagram of the TDA8708 analogue-to-digital converter.

The video amplifier features switchable AGC (automatic gain control) and clamping circuits. The AGC sets the upper video level (peak white); the clamping, the lower video level (base of sync pulse). As illustrated in Fig. 2, the peak white level produces the highest digital value, and the base of the sync pulse, the lowest digital value. The AGC and clamping sections receive information on the instantaneous drive level of the ADC via three comparators: one for the white level, one for the black level and one for the sync level. The AGC and the clamping logic each drive a pulsating direct current source that controls the video amplifier gain. The control current causes a voltage drop on the AGC capacitor connected to pin 25 of the TDA8708. The minimum and maximum video amplifier gains are 0.5 and 2.3 times respectively, corresponding to control voltage levels of 2.8 V and 4.0 V. As an option, the gain may be determined externally by omitting the AGC capacitor and applying a direct voltage instead. This, however, requires a fairly accurate temperature compensation circuit.

The gain of the internal amplifier is also controlled as a function of the lower video level: here, the voltage across the clamp capacitor at pin 24 is subtracted from the instantaneous video input voltage. A current limiting resistor, R_{PEAK} at pin 28, determines the level of the current diverted when the instantaneous level of the video signal exceeds the set limits. With $R_{PEAK} = 0\ \Omega$, the diverted current has a maximum level of 80 µA.

Table 2 lists the various possibilities of controlling the upper and lower video levels with the aid of logic levels applied to the GATE A and GATE B inputs of the chip.
In mode 1 (GATE A = GATE B = 1), the ADC output values are 255 for peak white and 0 for the base of the sync pulse. Mode 2 by contrast affords greater control over the conversion output values. As shown in Fig. 2, a positive pulse at the GATE A pin links the sync level to a value of 0. A positive pulse applied to the GATE B pin during the back porch sets the digital value of the top of the sync pulse to 64. The white level comparator is active all the time. Nominal levels of the video input signal produce a digital value of 213. This creates a safety margin of between 213 and 240. When the output value exceeds 240, the white level comparator reduces the gain of the video amplifier. This is done to reduce the risk of ADC overdrive to a minimum.

The analogue output, AN OUT (pin 19), of the video amplifier is connected to an external anti-aliasing low-pass filter. The maximum amplifier output current is limited to 2.5 mA, while the maximum output voltage is set to 1 V_{pp} at a nominal video input level of 1 V_{pp}. Table 3 lists a few additional characteristics relevant to the input circuit in the TDA8708.

The output signal of the external filter is fed back into the IC via the ADC IN pin. The ADC input may also be driven direct, provided the applied video signal has a voltage range of (V_{CCA}–1.6) V to (V_{CCA}–1.1) V. The input impedance of the ADC is about 50 MΩ,

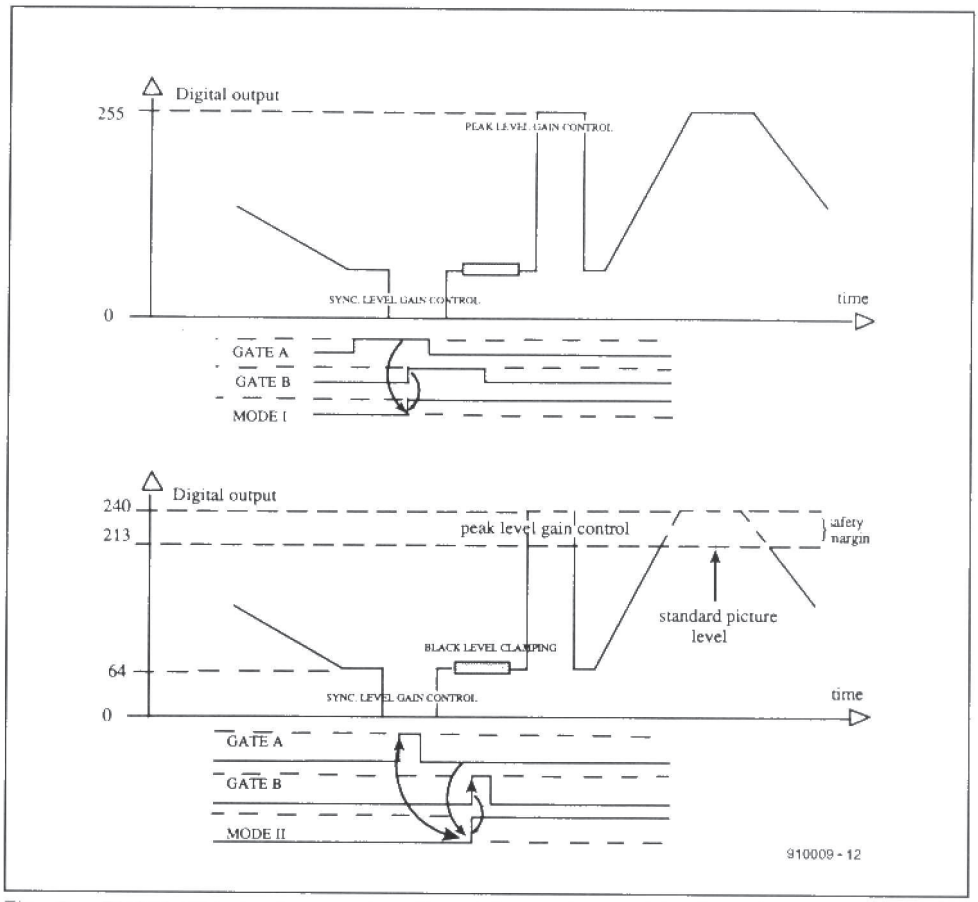

Fig. 2. Digital output value as a function of the analogue video input level in mode-1 (top drawing) and mode-2 (lower drawing).

Table 2. TDA8708 Mode Selection

GATE A B	Output	AGC	I_{CLAMP}	MODE
	<0	–2.5µA	I_{PEAK}	
1 1	0 - 255	–2.5µA	–2.5µA	1
	>255	I_{PEAK}	–2.5µA	
0 0	<240	0	0	
0 0	>240	0	I_{PEAK}	
1 0	<0	+2.5µA	0	
1 0	0 - 240	–2.5µA	0	2
1 0	>240	I_{PEAK}	0	
0 1	<64	+50µA	0	
0 1	64 - 240	–50µA	0	
0 1	>240	–50µA	I_{PEAK}	

Table 3. TDA8708 main technical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCA}	analogue supply voltage	4.5	5.0	5.5	V
I_{CCA}	analogue supply current	—	37	45	mA
—	VINx crosstalk	—	–60	–55	dB
G_d	Gain error	—	2	—	%
Φ_d	phase error	—	2	—	°
B	–3dB bandwidth	12	—	—	MHz
S/N	noise distance	60	—	—	dB
SVRR	supply voltage rejection	—	45	—	dB
G	Gain	–4.5	—	6.0	dB

Table 4. TDA8708 pin function description

Pin	Symbol	Description
1-4	D7 (MSB) - D4	Digital outputs, bit 7 (MSB) through bit 4
5	CL	Clock input
6	VCCD	Digital supply voltage +5 V
7	VCCO	TTL output supply voltage +5 V
8	DGND	Digital ground
9	OF	Output format and chip enable (3-state)
10-13	D3 - D0 (LSB)	Digital outputs, bit 3 through bit 0 (LSB)
14,15	I0, I1	Video input channel selection
16-18	VIN0 - VIN2	Analogue video inputs 1, 2, 3
19	ANOUT	Analogue voltage output
20	ADCIN	ADC input
21	DEC	Decoupling capacitor for ADC
22	VCCA	Analogue supply voltage +5 V
23	AGND	Analogue ground
24	CLAMP	clamp capacitor
25	AGC	AGC capacitor
26,27	GATEB, GATEA	clamping and sync level control
28	RPEAK	current limit for AGC

and the input capacitance is as low as 1 pF.

The maximum clock rate of the ADC inside the TDA8708 is 30 MHz. The timing is illustrated in Fig. 4: the analogue input voltage is measured 2 ns (t_{su}) after the leading edge of the clock signal has exceeded the reference level of 1.5 V. The previous digital word remains on the outputs for another four to six nanoseconds, and is replaced by the new value after a delay t_d (16 to 20 ns).

The digital outputs of the ADC, D0 through D7, have a 20 µA current sinking or sourcing capability. The digital word is supplied either in binary form (with pin OF not connected) or as a two's complement value (with pin OF at logic 0). The ADC outputs are switched to high-impedance when the OF input is made logic high. Finally on the ADC, Table 4 provides the descriptions of the signals associated with the IC pins.

TDA8702 digital-to-analogue converter

This IC is of a much simpler layout than its counterpart — see the block diagram in Fig. 3. The pinning of the DAC is given in Table 5.

The digital data applied to the TDA8702 is accepted at the D0 through D7 inputs, which are TTL-compatible. The data are buffered by an input interface before they are loaded into a register. As shown in the block diagram, the register drives eight constant-current sources that translate the digital value into a corresponding analogue quantity, in this case, a current. Each digital output causes a current of about 85 µA to flow through the 75-Ω resistor. This in turn causes a voltage drop of about 6.3 mV with respect to the positive analogue supply voltage, V_{CCA}, provided the load impedance is relatively high. Table 6 provides information on the DAC output level for load impedances of 10 kΩ and 75 Ω.

While the output voltage (w.r.t. V_{CCA}) at the VOUT pin is proportional to the digital input value, the VOUTN pin supplies an inverted output signal. The signals at VOUT and VOUTN are typically coupled out via an electrolytic capacitor of 68 µF to 100 µF. Each of these introduces a voltage drop,

$$V_c = \frac{V_{OUT} \times R_L}{R_L + 75\Omega}$$

where R_L is the load impedance.

The circuit in Fig. 6 shows the two video outputs connected to a differential amplifier. This may be done to increase the suppression of hum and noise on the ADC supply voltage. A suggestion for a simple transistor-based buffer amplifier is given in Fig. 6.

Finally, a few notes on the timing of the TDA8702. As shown in Fig. 7, the DAC is transparent while CL (clock) is held logic low. Transparent means that the DAC follows the changes of the digital input signal. The

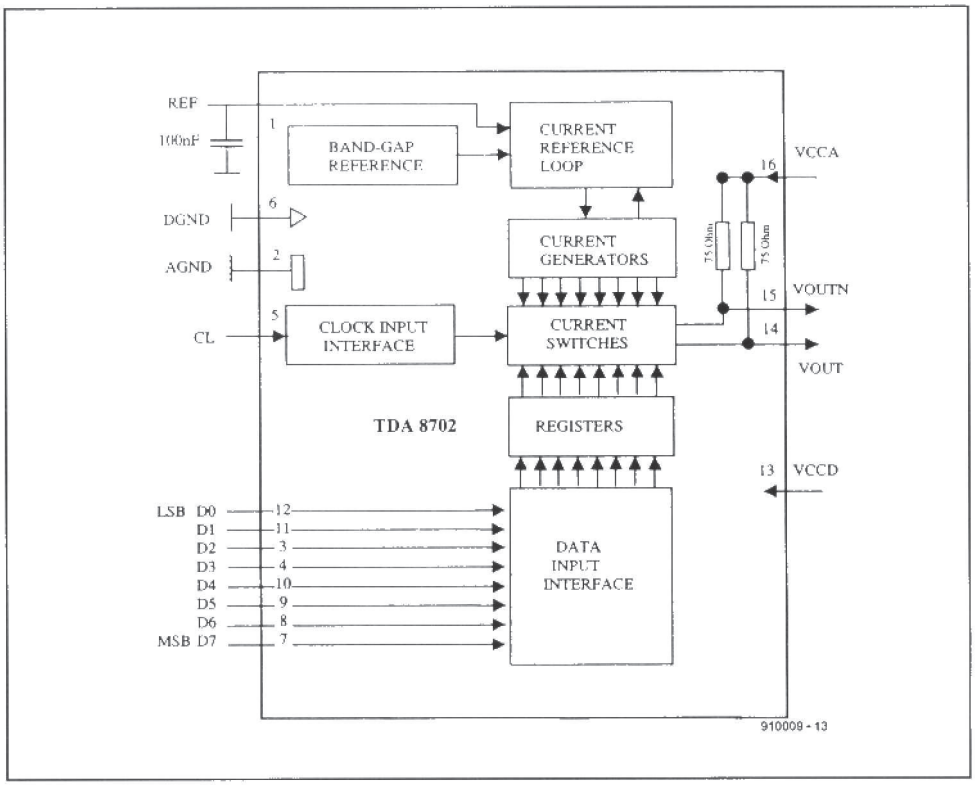

Fig. 3. Block diagram of the TDA8702 digital-to-analogue converter.

Table 5. TDA8702 pin function description

Pin	Symbol	Description
1	REF	Reference voltage source decoupling
2	AGND	Analogue ground
3,4	D2,D3	Digital video inputs bits 2, 3
5	CL	Clock input
6	DGND	Digital ground
7-10	D7-D4	Digital video inputs bit 7 (MSB) through 4
11,12	D1,D0	Digital inputs bit 1, bit 0 (LSB)
13	VCCD	Digital supply voltage +5 V
14	VOUT	Analogue video output
15	VOUTN	Inverted analogue video output
16	VCCA	Analogue supply voltage +5 V

Table 6. TDA 8702 output loading data

Code	Binary	Output voltage at Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT} [V]	V_{OUTN} [V]	V_{OUT} [V]	V_{OUTN} [V]
000	000 000 00	0	–1.6	0	–0.8
001	000 000 01	–0.006	–1.594	–0.003	–0.797
...					
128	100 000 00	–0.8	–0.8	–0.4	–0.4
...					
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

TDA8702 latches the current digital value when the clock signal reaches a value of 1.3 V on the leading edge. To ensure that the output voltage is stable until the trailing edge of the clock signal, the input data must be stable at least 0.3 ns before, and 2 ns after, the threshold is reached. Table 7 lists the main technical characteristics of the TDA8702.

Next month's final instalment of this article will describe a construction project based on the TDA8708 and TDA8702.

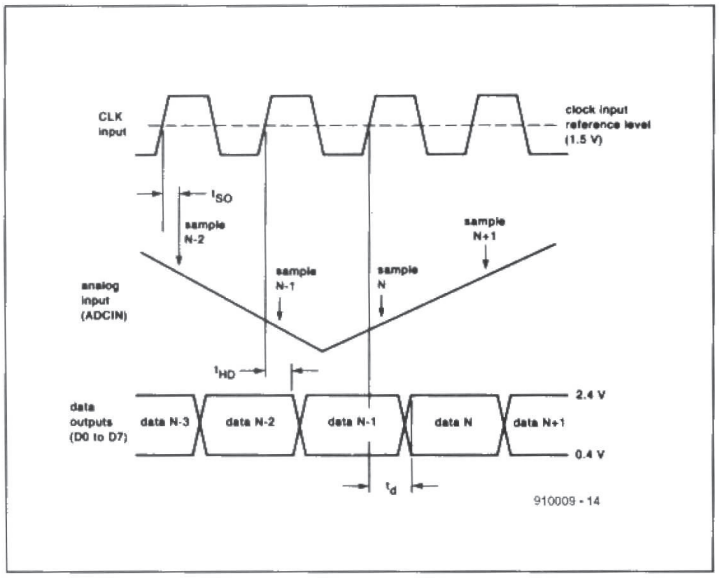

Fig. 4. TDA8708 data conversion timing.

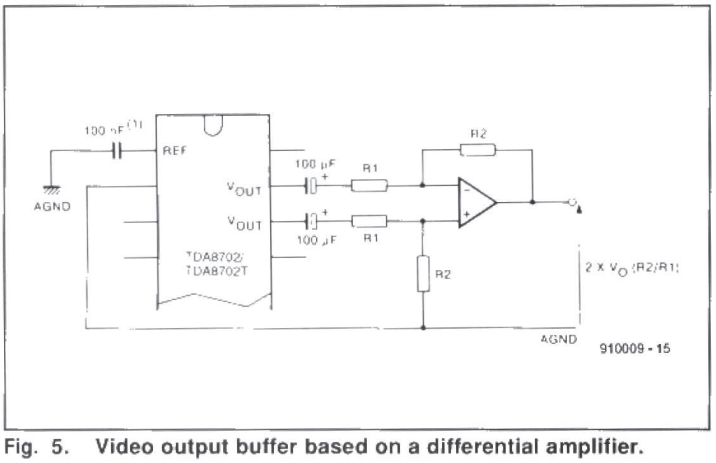

Fig. 5. Video output buffer based on a differential amplifier.

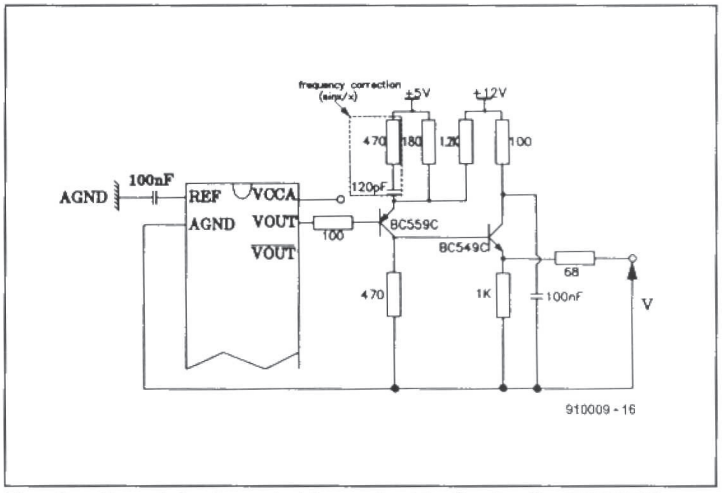

Fig. 6. Transistor-based video output buffer for the TDA8702.

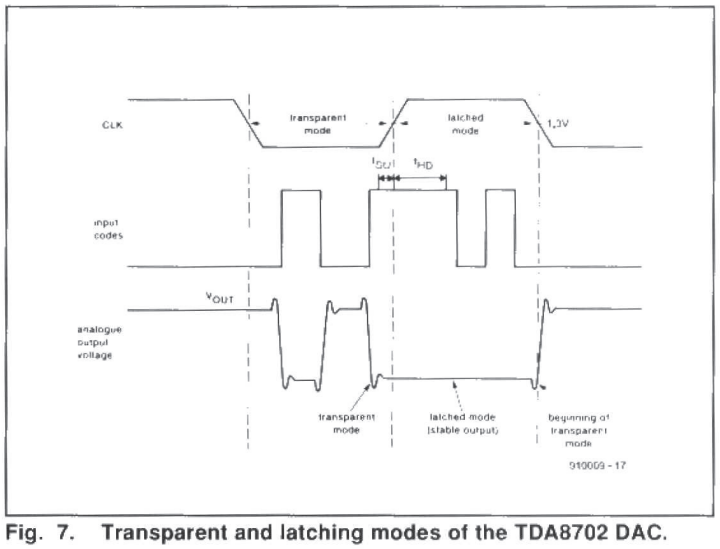

Fig. 7. Transparent and latching modes of the TDA8702 DAC.

Table 7. TDA8702 main technical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCA}	Analogue supply voltage	4.5	5.0	5.5	V
I_{CCA}	Analogue supply current	-	26	32	mA
V_{CCD}	Digital supply voltage	4.5	5.0	5.5	V
I_{CCD}	Digital supply current	-	23	30	mA
$V_{OUT(N)}$	Output voltage (Z_L=10kΩ)	–1.45	–1.6	–1.75	V
	(Z_L=75Ω)	–0.72	–0.8	–0.88	V
V_{OFF}	Output offset	-	–3	–25	mV
$\Delta V_{OUT(N)}/\Delta T$	Temperature co-eff. V_{OUT}			200	µV/K
$\Delta V_{OFF}/\Delta T$	Temperature co-eff. V_{OFF}			20	µV/K
B_{3dB}	3-dB bandwidth of analogue output		150		MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
$Z_{OUT(N)}$	Output impedance		75		Ω
DLE	Differential linearity error			±0.5	LSB
ILE	Internal linearity error			±0.5	LSB
t_{su}	Data setup time	0.3			ns
t_{HD}	Data hold time	2.0			ns
t_{pd}	Propagation delay			1.0	ns
t_{s1}	Settling time 10-90%		1.1	1.5	ns
t_{s2}	Settling time ±1 LSB		6.5	8.0	ns